

REMARKS/ARGUMENTS

Reconsideration of the Application in view of the above amendments and the following remarks is respectfully requested.

The Examiner rejects Claims 1, 2, 8, 9 and 10 under 35 U.S.C. 103(a) as being unpatentable over Neukermans, et al. in view of Laor, et al. The Examiner states that Neukermans, et al. discloses a method of fabricating an optic switch using bonded silicon wafer substrates and that the method comprises forming a substrate 212 including some via holes through the substrate 212 which reads on fabricating a carrier wafer having a plurality of holes therethrough. The Examiner states that the front side of the wafer 162 is connected align with the substrate 212 having some via holes which reads on mounting a structure wafer to the carrier wafer in alignment relative to the plurality of holes in the carrier wafer. The Examiner states that etching the openings in the wafer 162 of the structure wafer from the back side to form a plurality of moving mirrors having hinges of Neukermans, et al. shows a plurality of rotatable mirror/microstructures arranged in an array connected to the frame by hinges 176 and gimbal portions 178 which reads on etching openings through the structure wafer at a location away from the plurality of holes in the carrier wafer to form a plurality of rotatable microstructures. The Examiner then refers to separating or removing the substrate 162 structure wafer from the substrate 212/carrier wafer and specifically refers to col. 17, lines 15-17 and Figure 15. The Examiner states the Neukermans, et al. fails to disclose a step of attaching permanent magnets to the structure wafer as a hole locations. The Examiner states the Laor, et al. discloses a method of fabricating optical switching apparatus comprising the step of attaching permanent magnets to the carrier wafer. The Examiner states that both Neukermans, et al. and Laor, et al. are concerned with the method of fabricating optical switching apparatus having micromirrors, one skilled in the art would have found it obvious to modify Neukermans, et al. method by adding the step of attaching permanent magnets to the structure wafer at the locations

of the holes in the carrier wafer in view of Laor, et al. because Laor, et al. states that magnets are utilized to position the central mirror surface to a selected orientation thus eliminating undesirable oscillation under external shock or other condition.

We cannot agree. First of all, at col. 15, line 15-17 of Neukermans, et al., referred to by the Examiner, it recites: "...torsional scanners are preferable fabricated by micromachining single crystal silicon using Simox, silicon on insulator or bonded wafer substrates.". The term "bonded wafers substrates" referred to by the Examiner are oxide bonded wafers, which are made by thermally bonding two silicon wafers together and then thinning one of the two bonded wafers to the desired thickness either by grinding and polishing or by the "smart crack" process. This is very different than the mounting of the structure wafer to the carrier wafer recited in Claim 1. In Claim 1, the last step is removing the carrier wafer from the structure wafer, which is not the same as utilized in Neukermans, et al. In order to further emphasize this, Claim 1 has been amended to recite that the structure wafer is temporarily mounted to the carrier wafer, in sharp contrast to Neukermans, et al.

The step of mounting to the substrate 212 referred to by the Examiner is not a wafer stage processing step, the Examiner statements to the contrary notwithstanding. As recited in Neukermans, et al. at col. 18, lines 20-35, the torsional scanners 172 are preferably arranged into strips 222 which are then flip-chip bonded to a substrate 212 so that all the electrical connections to the strip are made between the strip and the substrate. Clearly, in order to mount the torsional scanners 172 to the strips and the substrate, they must be singularized, that is, diced from the wafer. Therefore, this is a post fabrication process used in making the array but not in forming the torsional devices themselves. Claim 1 clearly recites that all of the steps are for wafers, which, as is well known in the art, is a slice of silicon or other semiconductor material utilized to form a plurality of semiconductors or in this case, micromachined devices thereon. Therefore, the via holes in substrate 212 are not utilized to form the microstructures, they are utilized to mount them after they have already been formed. Furthermore, the term "via" utilized in Neukermans, et al. at the bottom of col. 18 is a term of art.

Enclosed herewith please find a definition of the term including two drawings thereof from the text PRINCIPLES OF CMOS VLSI DESIGN by Weste and Eshraghian. As can be seen from this definition, the holes formed to make the vias are not appropriate for accepting permanent magnets.

The Examiner statement that Figure 18b shows that the microstructures are enclosed/immobilized by substrate 224 is respectfully traversed. As clearly stated in col. 18, line 36 element 224 is a support frame, and not a substrate. With respect to the Examiner's referral to separate/removing the substrate 162 from the structural wafer 212, the Examiner has the process backwards. This is because the term "are separated [by] a distance e.g. from 40 to 50 microns, from the substrate 212 by spacers..." refers to the utilization of spacer elements whereas the term "removing" the carrier wafer from the structure wafer recited in Claim 1 is a physical act of separating one unit from another. These are very different meanings.

Neukermans, et al. relates to electrostatically deflected mirrors whereas Laor, et al. relates to magnetically deflected mirrors. The Examiner has not cited a rational for combining these two other than the fact that both relate to making micromirrors. In addition, Laor, et al. discloses at col. 6, lines 5-7 and Figure 3a mounting the magnets of a single mirror die after the mirrors are etched and the mirrors are singulated and released from the carrier wafer. In the present invention, the magnets are mounted to the wafer containing a plurality of micromirrors.

Claims 2, 8, 9 and 10 are dependent upon Claim 1 and are therefore patentable for the same reasons.

The Examiner rejects Claims 3-6, and 13-16 under 35 U.S.C. 103(a) as being unpatentable over Neukermans, et al. in view of Laor, et al. and further in view of Kane, et al. The Examiner states that unlike the claims of the present application Neukermans, et al. and Laor, et al. do not specifically disclose the steps of mounting the carrier wafer to a support wafer, forming a mask layer over a surface of the carrier

wafer/structure wafer patterning the mask layer to expose the carrier wafer, etching through the carrier layer by wet/dry etching to form a plurality of holes and releasing the carrier layer from the support wafer. The Examiner states that Kane, et al. discloses a method of making a low voltage micromirror which comprises the steps of mounting the carrier wafer to a support wafer, forming a mask layer over the surface of the carrier wafer/structure wafer, patterning the mask layer to expose the carrier wafer through the carrier layer by wet/dry etching to form a plurality of holes and releasing the carrier layer from the support wafer. The Examiner concludes that since Neukermans, et al., Laor, et al. and Kane, et al. are concerned with a method of fabricating optical switching apparatus having micromirrors, one skilled in the art would have found it obvious to incorporate the steps of Kane, et al. into Neukermans, et al. and Laor, et al. because Kane, et al. states that this method employs thin film deposition techniques and photolithography for readily forming the extreme thin switch, whereby the components thereof are substantially co-planar.

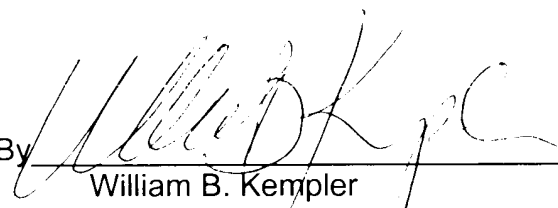
We cannot agree. First of all the "carrier wafer 9" referred to by the Examiner is, according to col. 10, lines 45 et seq a bottom electrode material sputtered or evaporated onto the substrate having a layer of titanium and a second layer of platinum. This is not a carrier wafer. Secondly, the mirror of the cited reference according to col. 9, last line through the top of col. 10 is deposited on the underside of the easily flexed support sheet 5. This is not a "structure wafer" as recited in the present Claim 1. Although Kane, et al. does disclose etching through a portion of the substrate 7, it does not show the fabrication utilizing two separate wafers and therefore cannot show removing the carrier wafer from the structure wafer. Furthermore, Claims 3-6 are dependent directly or indirectly from Claim 1 and Claims 13-16 are dependent directly or indirectly from Claim 11 and therefore patentable for the same reasons discussed above.

The Examiner found Claims 7 and 17 to be allowable but objected to as being dependent upon or rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. According, Claims 7 and 17 have been converted to independent claims.

Accordingly, Applicants believe the application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
Texas Instruments Incorporated

By

A handwritten signature in black ink, appearing to read 'W. B. Kempler', is written over a horizontal line.

William B. Kempler
Senior Corporate Patent Counsel
Reg. No. 28,228
Tel.: (972) 917-5452

Attachments

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Neil H. E. Weste

TLW, Inc.

Kamran Eshraghian

University of Adelaide



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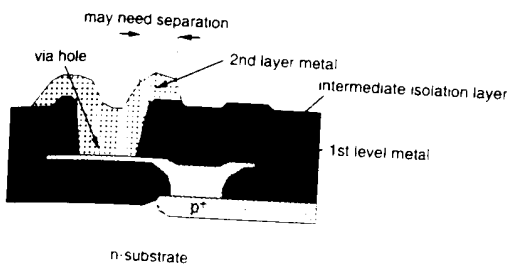


FIGURE 3.13 Two-level metal process cross section

metal layers. If some form of planarization is employed the second-level metal pitch can be the same as the first. As the vertical topology becomes more varied, the width and spacing of metal conductors has to increase so that the conductors do not thin and hence break at vertical topology jumps (*step coverage*).

Contacting the second-layer metal to the first-layer metal is achieved by a *via*, as shown in Fig. 3.13. If further contact to diffusion or polysilicon is required, a separation between the via and the contact cut is usually required. This requires a first-level metal *tab* to bridge between metal2 and the lower-level conductor. It is important to realize that in contemporary processes first-level metal must be involved in any contact to underlying areas. A number of contact geometries are shown in Fig. 3.14. Processes usually require metal borders around the via on both levels of metal although some pro-

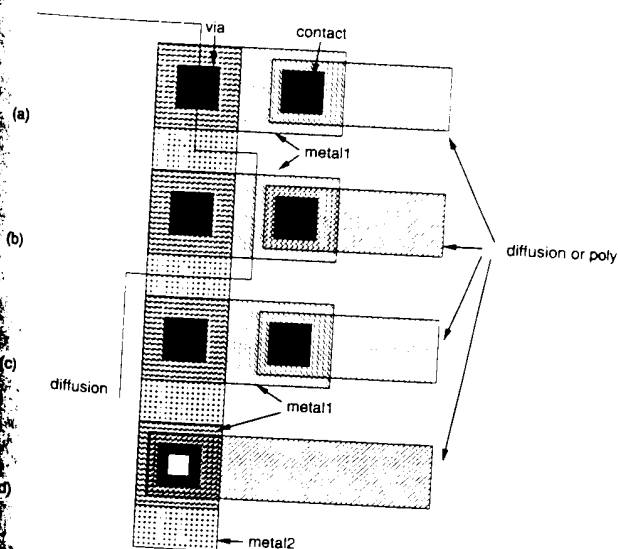


FIGURE 3.14 Two-level metal via/contact geometries